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Inventor(s): Chyan

Case: 15-6-9

Serial No.: 09/648164 ✓

Filing Date: August 25, 2000 ✓

Examiner: Dickey Group Art Unit: 2826

Title: Architecture For Circuit Connection Of A Vertical Transistor

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D. C. 20231

SIR:

INFORMATION DISCLOSURE STATEMENT
CERTIFICATION UNDER 37 CFR 1.97

Attached is a list of documents on form PTO-1449. It is requested that the examiner consider these documents and officially make them of record in accordance with the provisions of 37 CFR 1.97.

I certify that each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application. Copies of the listed documents are enclosed together with the search report that listed these documents.

In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Agere Systems Inc. Deposit Account No. 50-1735 as required to correct the error. Duplicate copies of this letter are enclosed.

Respectfully,

By Ferdinand M. Romano
Ferdinand M. Romano
Reg. No. 32,752

Date: 8-29-02

Att.
Information Disclosure Statement with attachment(s)

GP 2826
#101-1-D-5
9/24/02
S. M. H.

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